

REMARKS

Claim 21 is amended. Claims 23-28 are canceled. New claims 29-31 are added. No new matter is added as the originally-filed application supports the claims, for example, at page 8 and Fig. 6. Claims 21-22 and 29-31 are pending in the application.

Claims 21-22 stand rejected under 35 USC §102(e) as being anticipated by Ilg et al. (U.S. Patent No. 6,130,145).

The PTO and Federal Circuit provide that §102 anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). The corollary of this rule is that the absence from a cited §102 reference of any claimed element negates the anticipation. *Kloster Speedsteel AB, et al. v. Crucible, Inc., et al.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986).

Claim 21 recites a silicon-dioxide-containing dopant barrier layer against the metal-silicide layer. Ilg fails to teach or suggest, singularly or in any combination, a silicon-dioxide-containing dopant barrier layer against a metal-silicide layer. Accordingly, the art of record fails to teach a positively recited feature of claim 21. Claim 21 is allowable.

Claims 22 and 29-31 depend from independent claim 21, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are neither shown or taught by the art of record.

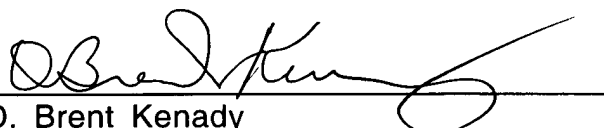
Further, Applicant herewith submits a duplicate copy of the Information

Disclosure Statement and Form PTO-1449 filed together with this application on June 4, 2001. No initialed copy of the PTO-1449 has been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 1-31-02

By: 
D. Brent Kenady
Reg. No. 40,045



EL844055781

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/875,501
Filing Date June 4, 2001
Inventor Klaus Florian Schuegraf, et al.
Assignee Micron Technology, Inc.
Group Art Unit 2815
Examiner E. Ortiz
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects,
and Wordline, Transistor Gate, and Conductive Interconnect Structures

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING
RESPONSE TO NOVEMBER 8, 2001 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions
and ~~strikeouts~~ indicate deletions.

21. (Amended) A conductive line comprising:
a polysilicon layer; ~~and~~
a metal-silicide layer against the layer of polysilicon, the metal-silicide layer
comprising a Group III dopant or a Group V dopant; and
a silicon-dioxide-containing dopant barrier layer against the metal-silicide
layer.

Please cancel the following claims:

23. Cancel.

24. Cancel.

25. Cancel.

26. Cancel.

27. Cancel.

28. Cancel.

Please add the following new claims:

29. (New) The conductive line of claim 21 wherein the silicon-dioxide-containing dopant barrier layer is elevationally above the metal-silicide layer.

30. (New) The conductive line of claim 21 wherein the metal-silicide layer comprises an elevationally uppermost surface relative to the polysilicon layer, and wherein the silicon-dioxide-containing dopant barrier layer is against the uppermost surface.

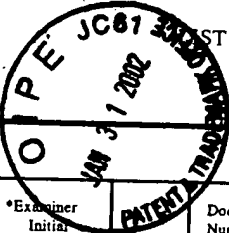
31. (New) The conductive line of claim 21 wherein the metal-silicide layer comprises an elevationally uppermost surface relative to the polysilicon layer, the uppermost surface having a width dimension, and wherein the silicon-dioxide-containing dopant barrier layer is against substantially the entire width of the uppermost surface.

-END OF DOCUMENT-

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Sheet 1 of 1

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
MI22-1741SERIAL NO.
Filed HerewithLIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
Klaus Florian Schuegraf et al.FILING DATE
Filed HerewithGROUP
Unknown

U.S. PATENT DOCUMENTS

JC896 U.S. PTO
09/07/501

06/04/01

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
EO	AA 5,425,392	06/95	Thakur et al.			
	AB					
	AC					
	AD					
	AE					
	AF					
	AG					
	AH					
	AI					
	AJ					
	AK					

FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Subclass	Translation	
					Yes	No
AL						

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

AK	Taishi Kubota et al.; "The Effect of the Floating Gate/Tunnel SiO ₂ Interface on FLASH Memory Data Retention Reliability"; 1994; 2 pages
AL	Shoue Jen Wang et al.; "Effects of Poly Depletion on the Estimate of Thin Dielectric Lifetime"; IEEE Electron Device Letters, Vol. 12, No. 11, November 1991; pp. 617-619.
AM	Klaus F. Schuegraf et al.; "Impact of Polysilicon Depletion in Thin Oxide MOS Technology"; 1993; pp. 86-88
AN	E. H. Snow et al.; "Polarization Phenomena and Other Properties of Phosphosilicate Glass Films on Silicon"; Journal of the Electrochemical Society, March 1966; pp. 263-269

EXAMINER

DATE CONSIDERED

12/2/01

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.